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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/965,283	09/25/2001	Randy P. Stanley	42390P12376	3844

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Thomas S. Ferrill
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER	
HOFFMAN, BRANDON S	

ART UNIT	PAPER NUMBER
2136	

DATE MAILED: 07/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/965,283	STANLEY, RANDY P.	
	Examiner	Art Unit	
	Brandon S. Hoffman	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3 and 5-34 are pending in this office action.

Rejections

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

3. Claims 1-3, 5-8, 10-27, 29-31, 33, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fung (U.S. Patent No. 5,396,635) in view of Watts, Jr. (U.S. Patent No. 6,848,054).

Regarding claims 1, 7, 20, 24, 27, and 30, Fung teaches an method/apparatus/ machine-readable medium, comprising:

- A computer readable medium (fig. 1, ref. num 15 and fig. 2);
- Detecting a user initiated event in a computing system (column 3, lines 12-21);
- A first integrated circuit having multiple states of performance including a first state of performance, a second state of performance higher than the first state of performance, and a third state of performance higher than the second state of performance, the first integrated circuit coupled to the computer readable medium (col. 2, lines 1-6 and fig. 8, 'sleep', 'doze', and 'on'); and

- A program stored in the computer readable medium to manage power consumption within the first integrated circuit, instructions associated with the program to directly transition the first integrated circuit from the first state of performance to the third state of performance based upon detecting a user initiated event (col. 3, lines 32-38).

Fung does not teach operating the integrated circuit at the third state of performance for a period of time followed by a predefined period of time where the integrated circuit operates at the second state of performance based upon the detection of the user initiated event, **wherein the second state is a thermal maximum performance state, and the third state is a maximum performance state**.

Watts, Jr. teaches operating the integrated circuit at the third state of performance for a period of time followed by a predefined period of time where the integrated circuit operates at the second state of performance based upon the detection of the user initiated event (fig. 1), **wherein the second state is a thermal maximum performance state, and the third state is a maximum performance state** (col. 6, lines 49-65).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine operating the IC at a third state for a predetermined period of time based on thermal failure characteristics, **wherein the second state is a**

thermal maximum performance state, and the third state is a maximum performance state, as taught by Watts, Jr., with the method/apparatus/medium of Fung. It would have been obvious for such modifications because a processing at high speeds produces a lot of heat and needs time to dissipate the heat. Speed is increased, but at a cost to the processor. Therefore, steps are needed to prevent processor damage.

Regarding claim 2, the combination of Fung as modified by Watts, Jr. teaches wherein the user event is defined by a programming environment within which the computing system is operating (see col. 3, lines 12-21 of Fung).

Regarding claim 3, the combination of Fung as modified by Watts, Jr. teaches wherein directly transitioning comprises transitioning without delay (see col. 3, lines 39-48 of Fung and col. 2, lines 29-32 of Watts, Jr.).

Regarding claim 5, the combination of Fung as modified by Watts, Jr. teaches wherein the computing system comprises a laptop computer (see fig. 6 of Watts, Jr.).

Regarding claim 6, the combination of Fung as modified by Watts, Jr. teaches wherein the computing system comprises a personal digital assistant (see col. 1, lines 22-23 of Fung).

Regarding claims 8 and 31, the combination of Fung as modified by Watts, Jr. teaches wherein the first state of performance comprises a first voltage level and a first operating frequency (see col. 6, lines 16-19 of Fung).

Regarding claims 10, 21, 25, 29, and 33, the combination of Fung as modified by Watts, Jr. teaches further comprising frequency regulation logic to change an operating frequency of the first integrated circuit, the frequency regulation logic to receive a signal from the program (see col. 6, lines 45-48 of Fung).

Regarding claims 11, 22, and 26, the combination of Fung as modified by Watts, Jr. teaches further comprising voltage regulation logic to change an operating voltage of the first integrated circuit, the voltage regulation logic to receive a signal from the program (see col. 6, lines 53-62 of Fung).

Regarding claims 12-14, the combination of Fung as modified by Watts, Jr. teaches wherein the instructions reside in a Basic Input Output System, an operating system, or an application software (see col. 5, lines 64-68 of Fung).

Regarding claim 15, the combination of Fung as modified by Watts, Jr. teaches wherein the first integrated circuit comprises a chip set (see col. 4, lines 40-50 of Fung).

Regarding claim 16, the combination of Fung as modified by Watts, Jr. teaches

wherein the first integrated circuit comprises a processing unit (see fig. 1, ref. num 4 of Fung).

Regarding claim 17, the combination of Fung as modified by Watts, Jr. teaches wherein the Basic Input Output System is to receive a notification signal from an operating system that the user event has occurred (see col. 5, lines 64-68 of Fung).

Regarding claim 18, the combination of Fung as modified by Watts, Jr. teaches wherein the program comprises an increasing state transition algorithm discrete from a decreasing state transition algorithm (see col. 3, lines 1-11 of Fung).

Regarding claim 19, the combination of Fung as modified by Watts, Jr. teaches wherein the program to transition the first integrated circuit to a next higher state of performance based upon an occurrence of a non-user event increasing utilization of the first integrated circuit over a preset threshold (see col. 3, lines 22-31 of Fung).

Regarding claim 23, the combination of Fung as modified by Watts, Jr. teaches operating the integrated circuit at the second state of performance for non-user initiated events (see fig. 8, the 'on' state only lasts for brief periods of time of Fung).

Regarding claim 34, the combination of Fung as modified by Watts, Jr. teaches wherein after the operating the integrated circuit at the third state of performance,

preventing the integrated circuit from operating in the third state of performance for one or more thermal gaps, wherein each thermal gap is of a predetermined period of time based on the heat dissipation capacity of the integrated circuit (see col. 11, lines 45-67 of Watts, Jr.).

Claims 9, 28, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fung (USPN '635) in view of Watts, Jr. (USPN '054), and further in view of Hawkins et al. (EP 0,708,398).

Regarding claims 9, 28, and 32, the combination of Fung as modified by Watts, Jr. teaches all the limitations of claims 7, 27, and 30, respectively, above. However, the combination of Fung as modified by Watts, Jr. does not disclose wherein the third state of performance comprises a second integrated circuit co-processing instructions with the first integrated circuit.

Hawkins et al. teaches wherein the third state of performance comprises a second integrated circuit co-processing instructions with the first integrated circuit (page 7, table I).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine a second IC co-processing instructions for a third state, as taught by Hawkins et al., with the apparatus/readable medium of Fung/Watts, Jr.. It

would have been obvious for such modifications because a second processor processing during a third state of performance provides full speed processing power (see page 7, lines 29-33 of Hawkins et al.). These arts are analogous because they are both limiting power based on certain events.

Response to Arguments

4. Applicant amends claims 1, 7, 20, 24, 27, and 30.

5. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brandon S. Hoffman whose telephone number is 571-272-3863. The examiner can normally be reached on M-F 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz R. Sheikh can be reached on 571-272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BH

AYAZ SHEIKH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100